

## BURST/PIPELINED EDO MEMORY DEVICE

### ABSTRACT

5 An integrated circuit memory device is designed for high speed data access and  
for compatibility with existing memory systems. An address strobe signal is used to latch  
a first address. During a burst access cycle the address is incremented internal to the  
device with additional address strobe transitions. A new memory address is only required  
at the beginning of each burst access. Read/Write commands are issued once per burst  
10 access eliminating the need to toggle the Read/Write control line at the device cycle  
frequency. Transitions of the Read/Write control line during a burst access will terminate  
the burst access, reset the burst length counter and initialize the device for another burst  
access. The device is compatible with existing Extended Data Out DRAM device  
pinouts, Fast Page Mode and Extended Data Out Single In-Line Memory Module  
15 pinouts, and other memory circuit designs. Additionally, a DRAM is provided having  
both pipelined and burst Extended Data Out modes of operation and the ability to switch  
between them. ^

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